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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,305	10/27/2000	Takaki Yoshida	YMOR:186	4222

27890 7590 10/24/2005

STEPTOE & JOHNSON LLP
1330 CONNECTICUT AVENUE, N.W.
WASHINGTON, DC 20036

EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,305	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-11,13,19 and 20* is/are pending in the application.

4a) Of the above claim(s) *5,6,10 and 11* is/are withdrawn from consideration.

5)☒ Claim(s) *7-9,13,19 and 20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050923*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 5, 6, 10 and 11, drawn to A fault detecting method comprising: weighting possible faults at physical sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults; providing fault coverage by identifying a fault coverage value from the sum of the weighted fault coverage of detected weighted possible faults, wherein said fault list is a weighted fault list with respect to all faults listed therein, and said fault coverage is a rate of fault coverage detected by the weighted fault list, classified in class 714, subclass 741.

II. Claims 7-9, 13, 19 and 20, drawn to A fault detecting method comprising: calculating a density of a mask pattern corresponding to mask information obtained from a layout device for laying out the semiconductor integrated circuit to which said fault list corresponds; calculating a likelihood of occurrence for each possible fault depending on the density of the mask pattern; weighting the arranged possible faults according to said calculated likelihoods of occurrence; arranging the possible faults in the fault list in order according to their likelihood of occurrence to create an ordered fault list; and detecting faults in said semiconductor integrated circuit by using the ordered fault list, wherein the fault list comprises data

about a likelihood of a fault occurring at a physical site, classified in class 714, subclass 732.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and Group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for weighting possible faults at physical sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults; providing fault coverage by identifying a fault coverage value from the sum of the weighted fault coverage of detected weighted possible faults, wherein said fault list is a weighted fault list with respect to all faults listed therein, and said fault coverage is a rate of fault coverage detected by the weighted fault list. In the instant case, invention Group II has separate utility such as for calculating a density of a mask pattern corresponding to mask information obtained from a layout device for laying out the semiconductor integrated circuit to which said fault list corresponds; calculating a likelihood of occurrence for each possible fault depending on the density of the mask pattern; weighting the arranged possible faults according to said calculated likelihoods of occurrence; arranging the possible faults in the fault list in order according to their likelihood of occurrence to create an ordered fault list; and detecting faults in said semiconductor integrated circuit by using the ordered fault list, wherein the fault list comprises data about a likelihood of a fault occurring at a physical site. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Roger W. Parkhurst on 9/15/2005 a provisional election was made with traverse to prosecute the invention of Group II, claims 7-9, 13, 19 and 20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 5, 6, 10 and 11 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Allowable Subject Matter

Claims 7-9, 13, 19 and 20 are allowed.

This application is in condition for allowance except for the following formal matters:

Claims 5, 6, 10 and 11 need to be cancelled.

Conclusion

This application is in condition for allowance except for the following formal matters:

Claims 5, 6, 10 and 11 need to be cancelled.

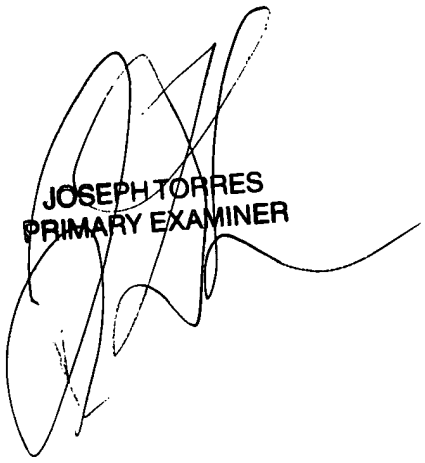
This is a RCE of applicant's earlier Application. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133